Wireless Power Controller CH247

Datasheet

Version: 1A

http://wch.cn

1. Overview

The CH247 is a wireless power controller which integrates a wireless charging transceiver module and small-signal decoding circuit, and it can easily implement various wireless charging solutions such as WPC Qi. Built-in PD controller and PD PHY transceiver. CH247 supports PD, BC and other fast charging protocols. It supports firmware upgrade via USB interface, no programmer required. CH247 integrates FSK/ASK generation, over-voltage protection, over-current protection, and over-temperature protection. It features high integration and streamlined peripherals. It can be widely used in designs such as wireless charging bases.

2. Features

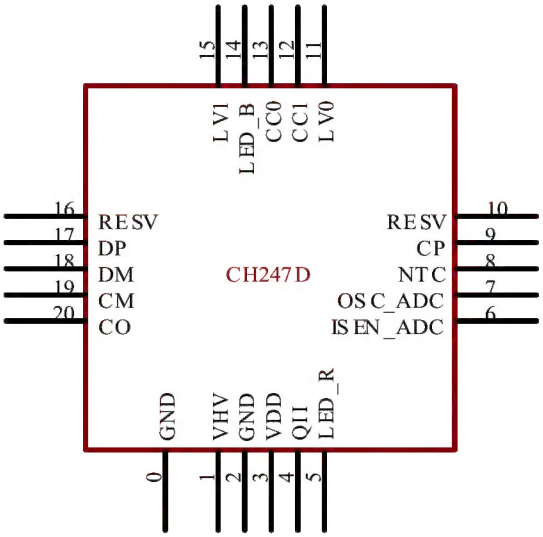
- 5V to 9V input voltage
- 5W, 7.5W, 10W, 15W wireless charging output power
- Power Tx design topologies MP-A2 and A11
- The input supports PD2.0, BC1.2 and other fast charging protocols
- Supports easy burning via USB interface
- Integrated over-voltage protection, under-voltage protection, over-temperature protection and over-current protection
- Integrated FSK/ASK generation
- Supports static and dynamic FOD detections
- Supports both half-bridge and full-bridge output modes
- Charging efficiency can be up to 80% or more
- 2 independent LED indicators

3. Applications

- Wireless charging base
- Wireless car charger
- Power bank

4. Pinouts

CH247D(QFN20_3*3) pinouts



5. Pin definitions

Pin No.	Pin Name	Pin Type	Description
0, 2	GND	Power	Ground
1	VHV	Power	High-voltage positive power supply, connects to an external 0.1uF decoupling capacitor.
3	VDD	Power	Internal LDO voltage output, connects to an external 0.1uFdecoupling capacitor
4	QII	Digital input	Wireless charging communication data input
5	LED_R	Digital output	Red LED indicator
6	ISEN_ADC	Analog input	Current detection pin
7	OSC_ADC	Analog input	Coil voltage detection pin
8	NTC	Analog input	External temperature detection pin
9	CP	Analog input	Positive input of internal op amp
11	LV0	Digital output	PWM0 output, VDD level
12	CC1	3-state I/O Analog I/O	Type-C CC1 input/output
13	CC0		Type-C CC0 input/output
14	LED_B	Digital output	Blue LED indicator
15	LV1	Digital output	PWM1 output, VDD level
17	DP	3-state I/O USB I/O	USB D+ signal
18	DM		USB D- signal
19	CM	Analog input	Negative input of internal op amp
20	CO	Analog output	Output of internal op amp
10, 16	RESV	-	Reserved. Can be customized.

6. Functional description of pins

6.1. VHV and VDD

The VHV pin supports high-voltage input, and the voltage ranges from 5V to 9V. The VDD pin is an output of internal LDO. It is required to connect 0.1uF decoupling capacitors close to these two pins respectively. The chip detects the VHV voltage in real time, and supports over-voltage protection and under-voltage

lockout.

6.2. QII

The QII pin is a QI message input pin. The chip decodes messages sent by the wireless power receiver in real time, so as to implement the output power adjustment and the wireless fast charging protocol handshake.

6.3. LED_R and LED_B

CH247 supports 2 independent LED indicators, and the lighting effects can be customized according to user needs. Active low by default. The red and blue LEDs are on for 2 seconds at the same time when powered on. The red LED is on when it is in standby mode. The blue LED breathes when charging, and it is fully on when fully charged. The red and blue LEDs flash rapidly at the same time when an abnormal condition occurs.

6.4. IESN_ADC

Input current measurement pin. The sampling resistance is 100mR. Mainly used for over-current protection and foreign object detection.

6.5. OSC_ADC

Coil voltage measurement pin. Mainly used for static foreign object detection and output power limitation based on Q-factor. Fine-tuning the voltage divider resistor of the OSC_ADC pin can change the static foreign object trigger sensitivity and the power limit when the coil is output at a long distance.

6.6. NTC

External NTC input detection pin. Used for over-temperature protection. The NTC pin needs an external fixed pull-up 5.1K resistor. 10K or 100K NTC is recommended (b=3950). By default, the firmware matches 100K NTC, which corresponds to a protection temperature of about 80°C. When the temperature exceeds this protection temperature, the charging stops. When the temperature drops below 60°C, the charging is turned on again. If the external NTC function is disabled, this pin needs to be connected to high level.

6.7. Bridge driver pins: LV0 and LV1

LV0 and LV1 are bridge driver pins which support half-bridge and full-bridge drive modes, and support duty cycle adjustment. The output frequency ranges from 110K to 145KHz.

6.8. CC0/CC1

Used for PD fast charging protocol handshake. CC0 and CC1 both have built-in 5.1KΩ pull-down resistors, no external resistors required. After powered on, a PD handshake with adapter is automatically generated, and they request for high voltage.

6.9. UDP/UDM

UDP and UDM are used for BC1.2 fast charging protocol handshake. A BC handshake with adapter is automatically generated.

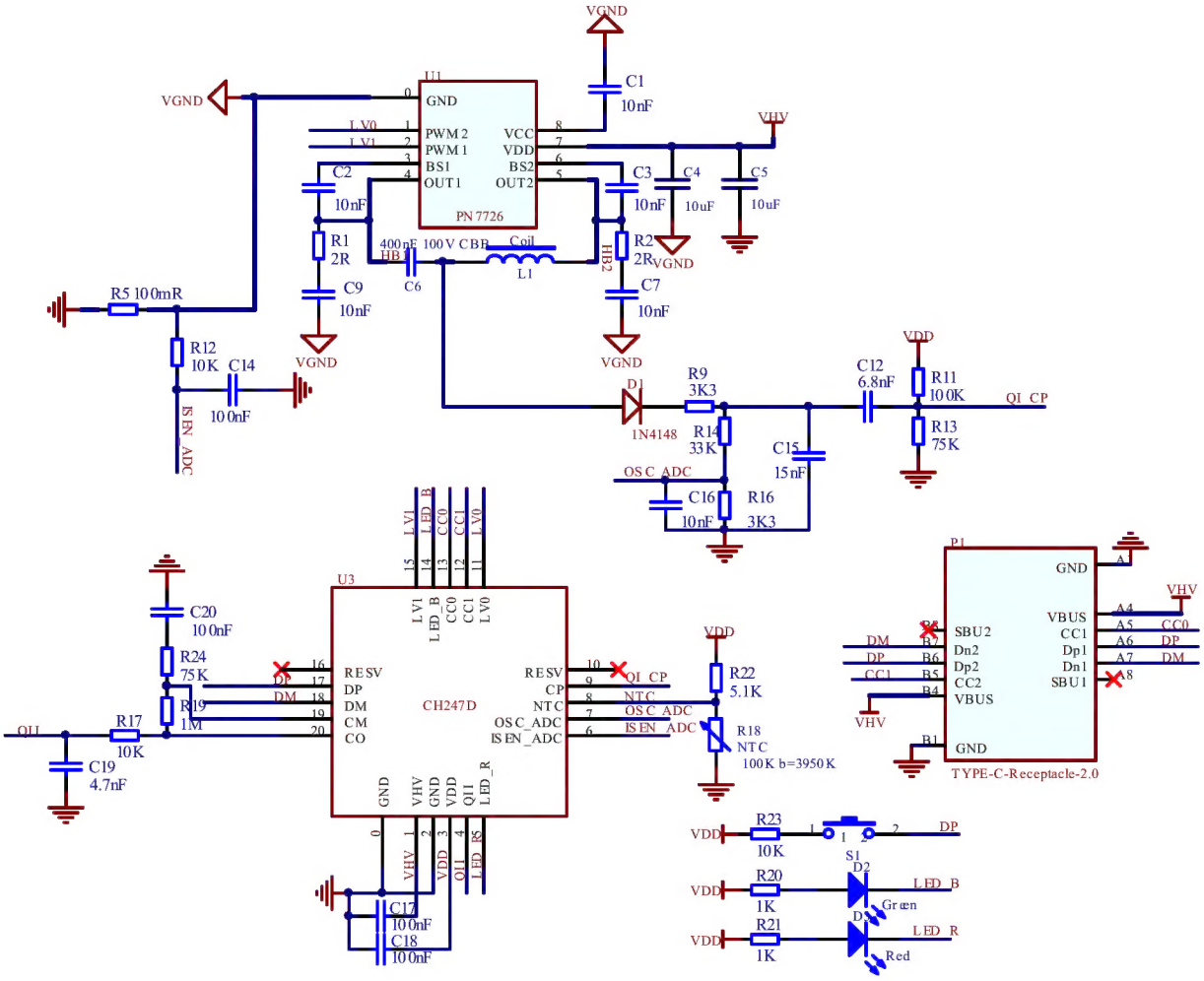
When powered on, if the UDP pin is pulled up, it enters USB burning mode, and the firmware can be upgraded on-board.

6.10. CP/CM/CO

Integrated op amp. CP is the positive input of op amp. CM is the negative input of op amp. CO is the output of op amp. This op amp is used for QI message decoding.

7. Application circuit for reference

CH247D circuit for reference

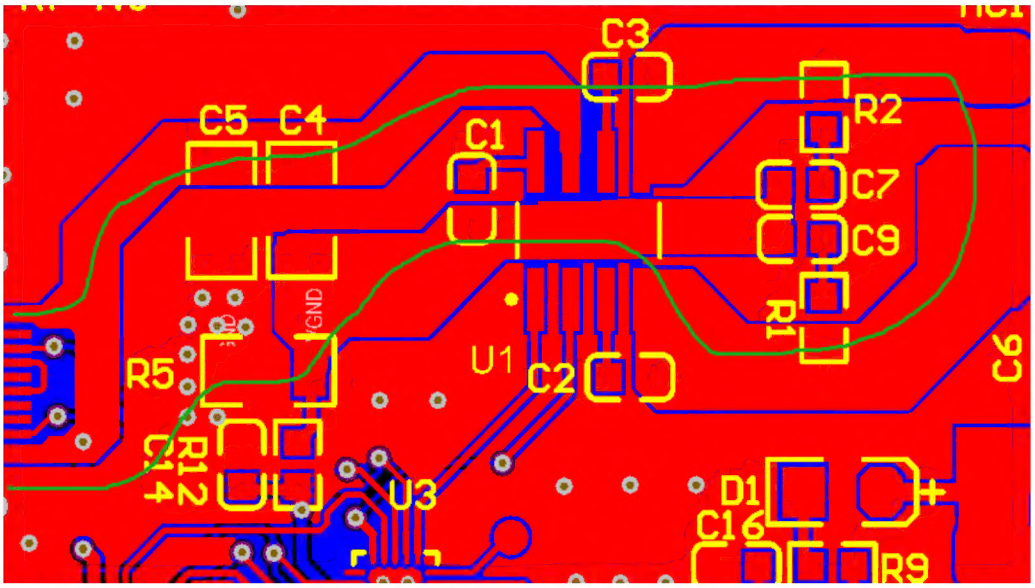


8. PCB design

LV0 and LV1 driver signal lines should be as short as possible, with few vias.

The current flows from the VHV network at the power input, passes through the U1 bridge, LC load, and R5 sampling resistor, eventually flows back to the GND network at the power input. Regarding PCB design, the loop should be as short as possible, and the traces should be as thick as possible. The green trace in the figure below is the high current loop. C4 and C5 are recommended to be placed at the current loop input.

CH247D(QFN20) PCB design for reference



9. Parameters

9.1. Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Symbol	Parameter description		Min.	Max.	Unit
TA	Operating ambient temperature	Fsys<40MHz (bLDO_CORE_VOL=0 is recommended)	-40	85	℃
		Fsys=48MHz (bLDO_CORE_VOL=1 is recommended)	-40	70	℃
TS	Storage ambient temperature		-55	125	℃
VDD	Voltage on internal USB and I/Os		-0.4	6.0	V
VHV	Power supply voltage (VHV connects to power, GND to ground)		-0.4	13.2	V
VIO	Voltage on input/output pins except Pin 9, Pin16		-0.4	VDD+0.4	V
VIOHV	Voltage on Pin 9 and Pin 16		-0.4	VHV+0.4	V

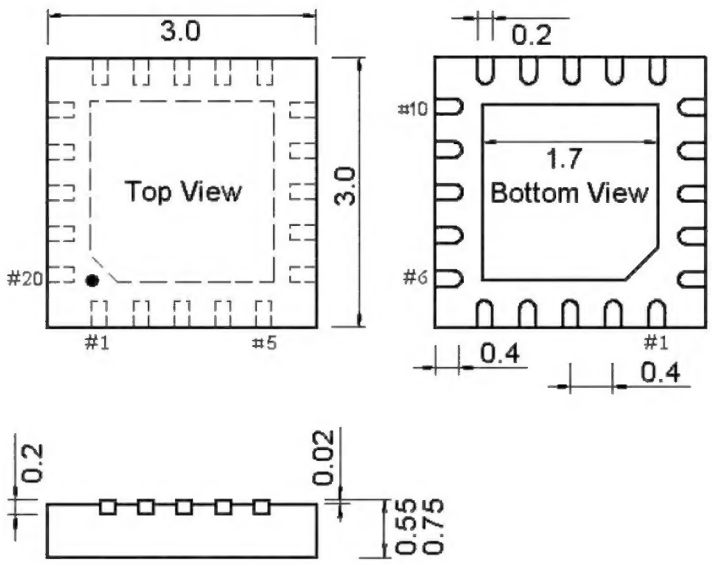
9.2. Electrical characteristics

Symbol	Parameter description	Min.	Typ.	Max.	Unit
VHV	Voltage on VHV12 pin	3.7	5	12.6	V
VDD	Output voltage on internal LDO	3.2	3.3	3.5	V
ICC48M3	Total supply current when Fsys=48MHz		6.0		mA
VIL3	Low level input voltage	0		0.8	V
VIH3	High level input voltage	2.0		VDD	V
VOL3	Low level output voltage (12mA sink current)			0.4	V
VOH3	High level output voltage (6mA source current)	VDD-0.4			V
Vovr	VHV over voltage reset threshold	13.2	14.5	15.8	V
Vpot	Power on reset threshold	2.2	2.3/2.8	3.0	V

9.3. Other parameters

Symbol	Parameter description	Min.	Typ.	Max.	Unit
NEPCE	Flash-ROM erase/program cycle endurance	10K	Not guaranteed 100K		times
TDR	Flash-ROM data retention	10			years
VESD	ESD voltage on I/O pins	4K	Not guaranteed 8K		V

10. Package information

Package	Body size	Lead pitch		Part No.
QFN20	3*3mm	0.40mm	15.7mil	CH247D

Note: All dimensions are in millimeters.